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ARENT FOX PLLC
1050 CONNECTICUT AVENUE, N.W.
SUITE 400
WASHINGTON, DC 20036

EXAMINER	
NGUYEN, TANH Q	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,462	TAKASE, HIROSHI	
	Examiner	Art Unit	
	Tanh Q. Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 14 recites the limitation "the bus" in line 5, and claim 16 recites the limitation "the bus" in line 5. There is insufficient antecedent basis for such limitation in the respective claims.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 4-6, 9-11, 15-16, 17-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 4 recites the limitation "wherein the transfer controller divides the data", which was not described in the specification.

Claim 9 recites the limitation "the direct memory access controller dividing the data", which was not described in the specification.

Claim 15 recites the limitation "reading data from the memory and dividing the read data", which was not described in the specification.

Claim 15 recites the limitation "dividing second digital data stored in the memory",

which was not described in the specification.

The specification only discloses a packet insertion circuit dividing the received data [page 12, lines 7-9], and does not disclose the transfer controller (DMA 27) dividing the transmit data read from the memory - as the specification discloses DMA 27 reading the transmit data from the memory in a state divided into data lengths corresponding to the isochronous packets [page 11, lines 1-5].

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-2, 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by **Maupin (USP 6,154,832)**.

6. As per claim 1, **Maupin** teaches a semiconductor device [14, FIG. 1] connected to a computer [10, FIG. 1] having a memory [16, 18, 20, FIG. 1], wherein the semiconductor device transfers data with a plurality of peripheral devices [col. 3, lines 46-48], the semiconductor device comprising:

a digital interface [30, FIG. 1] for controlling input and output of a digital signal;

an analog interface [26, FIG. 1] for controlling input and output of an analog signal; and

a transfer controller [22, FIG. 1] connected to the memory via a bus and to the digital and analog interfaces, wherein the transfer controller controls the transfer of data between the digital interface and the memory and between the analog interface and the memory [col. 4, lines 47-50].

7. As per claims 2, 7, 8, Maupin teaches the transfer controller being a DMA - hence teaches the data transferred between the analog interface and the memory (the block of data being transferred by the DMA controller) being divided into plural pieces of data having a predetermined data length (the block of data comprising a plural pieces of data having a predetermined data length);

a plurality of channels for the transfer controller to transfer data between the digital interface and the bus, wherein at least one of the channels is allocated for transmitting data and one of the channels is allocated for receiving data when the transfer controller transfers data between the analog interface and the bus [col. 4, lines 47-50];

the digital interface being one of a plurality of digital interfaces, and the analog interface being one of a plurality of analog interfaces [col. 3, lines 51-52].

8. Claims 1-4, 12-19 are rejected under 35 U.S.C. 102(e) as being anticipated by **Takenaka et al. (USP 6,772,354)**.

9. As per claim 1, **Takenaka** teaches a semiconductor device [60, FIGs. 1, 5] connected to a computer [1, FIGs. 1, 7; col. 1, lines 29-33] having a memory [13, 90, FIG. 7], wherein the semiconductor device transfers data with a plurality of peripheral devices [76, 77, 78, 81, 82, 83, FIG. 7; 30, 60, 110, 110, FIG. 1] the semiconductor device comprising:

a digital interface [61, FIG. 5] for controlling input and output of a digital signal;

an analog interface [66, FIG. 5] for controlling input and output of an analog signal; and

a transfer controller [61, 70, FIG. 5] connected to the memory via a bus [116, FIG. 5] and to the digital and analog interfaces, wherein the transfer controller controls the transfer of data between the digital interface and the memory and between the analog interface and the memory.

10. As per claims 2-4, Takenaka further teaches the data transferred between the analog interface and the memory being divided into plural pieces of data having a predetermined data length [data to be transmitted to a peripheral device being converted by the analog interface to digital data, the digital data being processed by the transfer controller (an IEEE-1394 interface) into a format compatible with the IEEE-1394 for transmission to a peripheral device over bus 116 [col. 10, lines 14-22], and the IEEE-1394 interface permitting isochronous communication whereby data of predetermined size are transmitted [col. 1, lines 23-28];

a packet insertion circuit [61, FIG. 5] connected to the analog interface and the transfer controller, wherein the packet insertion circuit divides the data the analog

interface receives from at least one of the peripheral devices into plural pieces of data having a predetermined data length, and adds a packet header and trailer data to each piece of data to generate a pseudo receive data packet [the IEEE-1394 interface performing packetization on the data for conversion into a format compatible with the IEEE-1394 [col. 10, lines 14-22], the IEEE-1394 interface permitting isochronous communication whereby data of a predetermined size are transmitted [col. 1, lines 23-28], and each isochronous packet having a packet header [FIG. 16; col. 21, line 56-col. 22, line 6] and trailer data [FIG. 16; col. 22, line 61], the transfer controller providing the pseudo receive data packets to the memory via the bus (packets being provided to the memory on the computer through bus 116);

the transfer controller dividing the data the analog interface transmits to at least one of the peripheral devices into plural pieces of data having a predetermined data length and adds a packet header to each piece of data to generate a pseudo transmit data packet [the IEEE-1394 interface performing packetization on the data for conversion into a format compatible with the IEEE-1394 [col. 10, lines 14-22], the IEEE-1394 interface permitting isochronous communication whereby data of a predetermined size are transmitted [col. 1, lines 23-28], and each isochronous packet having a structure of a common isochronous packet with a packet header [FIG. 16; col. 21, line 56-col. 22, line 6]];

11. As per claims 12-14, Takenaka teaches a method for controlling data transfer with a semiconductor device [60, FIGs. 1, 5] connected to a computer [1, FIGs. 1, 7; col. 1, lines 29-33] having a memory [13, 90], wherein the semiconductor device includes an

analog interface [66, FIG. 5], which transfers data with a plurality of peripheral devices [76, 77, 78, 81, 82, 83, FIG. 7; 30, 60, 110, 110, FIG. 1], and a transfer buffer [62, FIG. 5], the method comprising receiving data from at least one of the peripheral devices with the analog interface; storing the received data in the transfer buffer; dividing the stored data into plural pieces of data having a predetermined length; generating a pseudo data packet by adding a packet header and trailer data to each piece of data; and transferring the pseudo data packet to the memory [col. 10, lines 14-22; col. 1, lines 23-28; FIG. 16; col. 21, line 56-col. 22, line 6; col. 22, line 61].

Takenaka further teaches eliminating the packet header and the trailer data when storing the pseudo data packet in the memory [the pseudo packet being received in the IEEE-1394 interface [25, FIG. 7] of the computer [col. 15, lines 58], and data stored in the memory of the computer not including packet header and trailer data of the pseudo data packet [col. 13, line 61-col. 14, line 22; col. 9, lines 11-17];

the semiconductor device including a digital interface [61, FIG. 5] for transferring data with the peripheral devices, and a plurality of channels for transferring data between the digital interface and the bus [col. 19, lines 33-35], and the method further transferring the pseudo data packet to the memory from the buffer with at least one of the plurality of channels [col. 19, lines 33-35].

12. As per claims 15-16, Takenaka teaches a method for controlling data transfer with a semiconductor device [MD 1, FIG. 7] connected to a computer [STR 60, FIG. 5] having a memory [62, FIG. 5] for storing data, wherein the semiconductor device includes an analog interface [15, 19, FIG. 7], which transfers data with a plurality of

peripheral devices [16, 17, 18, 27, 20, 21, FIG. 7], and a transfer buffer [13, 90, FIG. 7], the method comprising:

reading data from the memory and dividing the read data into plural pieces of data having a predetermined length [col. 10, lines 16-22; col. 1, lines 23-28];

generating a pseudo data packet by adding a packet header to each piece of data [FIG. 16; col. 21, line 56-col. 22, line 6];

transferring the pseudo data packet to the transfer buffer (transferring packet from STR 60, FIG. 5 to MD 1, FIG. 7 to be stored in the transfer buffer [col. 15, lines 54-58]);

eliminating the packet header from the pseudo data packet to store the data in the transfer buffer [interface 25, FIG. 7 receiving data transferred over bus 116 [col. 15, lines 54-58], interface 25 implicitly capable of receiving audio data and decoding their packets - as is the case with interface 61, FIG. 5 [col. 9, lines 11-17]; furthermore, as the transfer buffer [13, 90, FIG. 7] stores data from Din [20, FIG. 7], Ain [18, 19, FIG. 7] in digital form, the digital form not including an IEEE-1394 packet header, the data stored from a pseudo data packet header in the transfer buffer is implicitly stored without the packet header]; and

reading the data from the transfer buffer and transmitting the read data to at least one of the peripheral devices with the analog interface (data recorded on the transfer buffer being transmitted to D/A converter to be processed and outputted to an audio output or a headphone).

Takenaka further teaches the semiconductor device includes a digital interface

[22, FIG. 7] for transferring data with the peripheral devices [20, 21, FIG. 7], and a plurality of channels for transferring data between the digital interface and the bus [col. 19, lines 33-35], the method further comprising transferring the pseudo data packet to the transfer buffer from the memory with at least one of the plurality of channels [col. 19, lines 33-35].

13. As per claims 17-19, Takenaka teaches a method for controlling data transfer with a semiconductor device [STR 60, FIG. 5] to a computer [MD 1, FIG. 7] having a memory [13, 90, FIG. 7], wherein the semiconductor device is connected to the memory via a system bus [116, FIG. 5, FIG. 7] and includes an analog interface [66, FIG. 5], a first transfer buffer [62, FIG. 5], and a second transfer buffer [61, FIG. 5], wherein the analog interface transfers data with a plurality of peripheral devices [76-79, 81-83, FIG. 5], the method comprising:

receiving analog data from at least one of the peripheral devices and converting the analog data to first digital data with the analog interface [67, FIG. 5]; storing the first digital data in the first transfer buffer [62, FIG. 5]; dividing the first digital data into plural pieces of data having a predetermined length when transferring the stored first digital data to the memory; generating a pseudo receive data packet by adding a packet header and trailer data to each piece of the divided first digital data; transferring the pseudo receive data packet to the memory via the system bus [col. 10, lines 14-22; col. 1, lines 23-28; FIG. 16; col. 21, line 56-col. 22, line 6; col. 22, line 61];

dividing second digital data stored in the memory into plural pieces of data having a predetermined data length [col. 10, lines 16-22; col. 1, lines 23-28]; generating

a pseudo transmit data packet by adding a packet header to each piece of the divided second digital data [FIG. 16; col. 21, line 56-col. 22, line 6]; transferring the pseudo transmit data packet to the second transfer buffer via the system bus (transferring packet from MD 1, FIG. 7 to STR 60, FIG. 5 to be stored in the second transfer buffer [col. 15, lines 54-58]);

eliminating the packet header from the pseudo transmit data packet to store the second digital data in the second transfer buffer [col. 9, lines 11-17]; and

converting the second digital data stored in the second transfer buffer [61, FIG. 5] to analog data [68, FIG. 5] and transferring the analog data to at least one of the peripheral devices [81-83, FIG. 5] with the analog interface [66, FIG. 5].

Takenaka further teaches the semiconductor device including a digital interface [61, FIG. 5] for transferring data with the peripheral devices and a plurality of channels to transfer data between the digital interface and the system bus, the method further comprising transferring the pseudo receive data packet from the first transfer buffer to the system bus with at least one of the plurality of channels [col. 19, lines 33-35];

eliminating the packet header and the trailer data when storing the pseudo receive data packet in the memory [interface 25, FIG. 7 receiving data transferred over bus 116 [col. 15, lines 54-58], interface 25 implicitly capable of receiving audio data and decoding their packets - as is the case with interface 61, FIG. 5 [col. 9, lines 11-17]; furthermore, as the transfer buffer [13, 90, FIG. 7] stores data from Din [20, FIG. 7], Ain [18, 19, FIG. 7] in digital form, the digital form not including an IEEE-1394 packet header or trailer data, the data stored from a pseudo data packet header in the transfer

buffer is implicitly stored without the packet header or trailer data].

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Takenaka et al.** in view of **Ghodrat et al. (USP 6,425,021]**.

Takenaka disclosed the invention except for the memory including a context program, and generating a pseudo transmit data packet including generating the pseudo transmit data packet in accordance with the context program.

Ghodrat teaches context programs directing the operation of the controller [col. 4, lines 28-29], and context programs being configured to include packet headers when moving packets into buffers [col. 5, lines 18-20].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to generate a pseudo transmit data packet in accordance with the context program, as is taught by Ghodrat, in order to direct the operation of the controller.

Allowable Subject Matter

16. Claims 5-6 are objected to as being dependent upon a rejected base claim, but

would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if applicant can point out the support for the limitation "wherein the transfer controller divides the data" recited in claim 4.

17. Claims 9-11 would be allowable if applicant can point the support for the limitation "the direct memory access controller dividing the data" recited in claim 9 - as the prior art does not teach a packet elimination circuit connected to the direct memory access controller and the AV interface to eliminate the packet header from the pseudo transmit data packet when the direct memory access controller transfers the pseudo transmit data packet to the AV interface; and a packet insertion circuit connected to the AV interface and the direct memory access controller, wherein the packet insertion circuit divides the data the AV interface receives from at least one of the peripheral devices into plural pieces of data having a predetermined data length and adds a packet header and trailer data to each piece of data to generate a pseudo receive data packet.

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tanh Quang Nguyen whose telephone number is (571) 272-4154 and whose e-mail address is tanh.nguyen36@uspto.gov. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici, can be reached on (571) 272-4083. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306

for After Final, Official, and Customer Services, or (571) 273-4154 for Draft to the Examiner (please label "PROPOSED" or "DRAFT").

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06/25/2005

TQN
June 25, 2005